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Low-Temperature Molecular Vapor Deposition of Ultrathin Metal Oxide Dielectric for Low-Voltage Vertical Organic Field Effect Transistors

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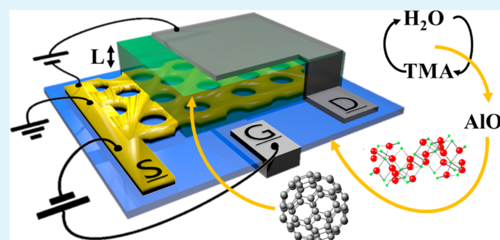
Supporting Information

ABSTRACT: We demonstrate a low-temperature layer-by-layer formation of a metal-oxide-only (AlO_x) gate dielectric to attain low-voltage operation of a self-assembly based vertical organic field effect transistor (VOFET). The AlO_x deposition method results in uniform films characterized by high quality dielectric properties. Pin-hole free ultrathin layers with thicknesses ranging between 1.2 and 24 nm feature bulk dielectric permittivity, ε_{AlOx}, of 8.2, high breakdownfield (>8 MV cm^{-1}), low leakage currents (<10^{-7}A cm^{-2} at 3MV cm^{-1}), and high capacitance (up to 1 μF cm^{-2}). We show the benefits of the tunable surface properties of the oxide-only dielectric utilized here, in facilitating the subsequent nanostructuring steps required to realize the VOFET patterned source electrode. Optimal wetting properties enable the directional block-copolymer based self-assembly patterning, as well as the formation of robust and continuous ultrathin metallic films. Supported by computer modeling, the vertical architecture and the methods demonstrated here offer a simple, low-cost, and free of expensive lithography route for the realization of low-voltage ($V_{GS/DS} \leq 3$ V), low-power, and potentially high-frequency large-area electronics.



KEYWORDS: *vertical field effect transistors, oxide dielectrics, self-assembly, thin films, vapor-deposition, flexible, conjugated polymers, organic molecules*

INTRODUCTION

Low-power and low-voltage operation is central to organic field effect transistors (OFETs), the key enabling elements in the realization of plastic-based electronics. With the potential advantage of low-cost and large-area fabrication amenability, flexible, thin, and lightweight structure, OFETs are expected to be integrated in a variety of applications including RFID tags,[1] flexible active matrix displays,[2] sensor arrays,[3] and disposable memory devices.[4] However, presently, the inherent low mobility of organic semiconductors (OSCs), compared to that of their inorganic counterparts, dictates high operating voltage and high power consumption, both of which are scarce in the typical off-grid applications. Intense research efforts aiming to overcome these limitations involve identifying new OSCs[5] and improved OSC morphologies,[6] controlling the interface chemistry of the gate dielectric,[7] varying structural parameters (downscaling),[8] and adopting different OFET architectures.[9−17] The patterned electrode vertical OFET (PE-VOFET), whose architecture is schematically shown in Figure 1i, is one such architecture. It offers the advantage of precise control and ease of downscaling of device critical dimensions, namely, the channel length, while remaining compatible with large area manufacturing.[13,18] Its inherent short channel length counterbalances the OSCs' low mobility[9,19] and facilitates low-power operation. Regardless, the gate bias range required to switch the device between the on and off states with standard 100 nm SiO_2 gate dielectric is typically large. In this work, we introduce an ultrathin, sub-10-nm thick, AlO_x-only gate dielectric, using a method that belongs to the family of layer by layer self-assembly methods.[20] We demonstrate the integration of the deposition process with the block-copolymers self-assembly based PE-VOFET structure formation, as illustrated in the fabrication process flow in Figure 1a−h. Particularly significant is the pinhole free film structure which facilitates reliable use of high capacitance elements for large-area applications and the low-temperature deposition which confers compatibility with typical flexible substrates. Finally, we show that the above combination of design and processes facilitates realization of low-power, low-voltage, and potential high frequency devices that drive high current density through low-cost fabrication and for large-area and flexible electronics.

The gate dielectric capacitance of metal-oxide-semiconductor based transistors is described by the equation $C = \varepsilon_0\varepsilon_r/d$, where

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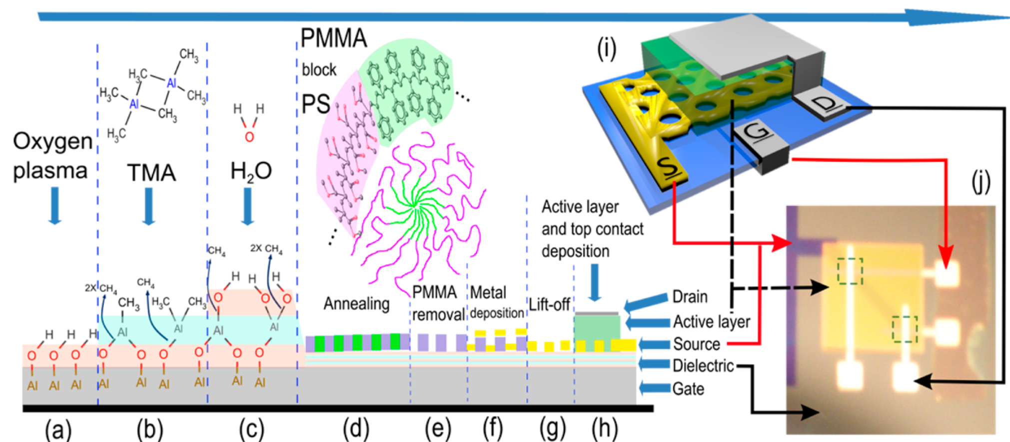


Figure 1. Schematic flow of the PE-VOFET fabrication process. Left to right: (a) Remote plasma surface (Al) functionalization, (b and c) layer by layer deposition (H_2O and TMA) of AlO_x, (d) block-copolymer self-assembly into vertical cylindrical structures based on the PS-b-PMMA different blocks immiscibility, (e) mask preparation, (f) metal deposition, (g) patterned electrode formation through lift-off process, (h) active layer and top contact (drain) deposition, and (i) 3D illustration of the PE-VOFET architecture. (j) Image of the structured back gate VOFET architecture.

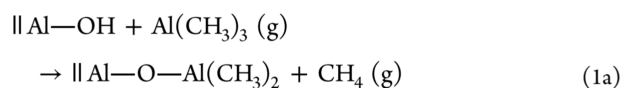
ε_0, ε_r, and d are the vacuum permittivity, the relative permittivity and the dielectric layer thickness, respectively. Hence, increased capacitance is pursued by adopting ultrathin solid-state dielectric layers, and by employing materials with dielectric constants higher than that of the traditional thermally grown SiO_2 (ε_r = 3.9). Organic-only dielectric layers, such as BCB,[21] PVA,[22] PMMA,[23] or parylene C,[24] have attractive structural properties; yet these materials have low dielectric constants and impose fabrication limitations due to difficulties involving surface functionalization. Oxide dielectrics, on the other hand, are advantaged with relatively high dielectric constants and their surface can be readily functionalized by a variety of polymers, Self-Assembled-Monolayers (SAMs) or other reactive molecules. Among the various methods to obtain oxide dielectrics, the more common ones are sol−gel deposition,[25] metal anodization,[26,27] plasma-induced ultrathin oxide layer functionalized with a judicial choice of SAMs,[28] and the layer-by-layer self-assembly process known as atomic layer deposition (ALD).[29] However, obtaining large-area, pinhole free films with low leakage currents in an oxide dielectric, so far requires use of thick oxides or the additional use of organic layers (polymer/SAMs) for the ultrathin oxides.[28] Consequently, the overall capacitance dramatically decreases. Here we describe a layer by layer self-assembly process that is somewhat different to the common ALD process using molecular vapor deposition tool (MVD100E by Applied Microstructures, Inc.). The differences in the process result in a modified, oxygen rich, AlO_x stoichiometry that is also associated with other electrical attributes. Those are the reliable, sub 10 nm pinhole free cm^2-scale layers, the bulk dielectric constant, ε_{AlOx}, which equals 8.2, and the improved insulating properties: High breakdown field (>8 MV cm^{-1}), low leakage currents (<10^{-7} A cm^{-2} at 3 MV cm^{-1}), and high capacitance (up to 1 μF cm^{-2}). It is worth noting that the nondestructive low temperature process incorporated here to form the gate dielectric of the PE-VOFET is independent of the substrate material and thus compatible with various architectures and substrates, including flexible ones.

■ RESULTS AND DISCUSSION

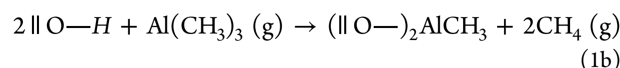
Like other layer-by-layer self-assembly processes, the ALD and its modifications are typically used for the formation of highly uniform SAMs employing organo-functional molecules. These are commonly utilized for the purpose of traps passivation,[7] free energy alignment, or energy levels alignment.[30] Here, employing water and the metalorganic molecule trimethylaluminium (TMA) as reactants, facilitates a layer-by-layer formation of AlO_x. These coupled reactants, considered ideal for either low[31,32] or high temperature ALD process because of their reactivity and process stability,[33] are of at least similar quality when prepared using the low temperature altered ALD process as described here.

The process chemistry of AlO_x monolayer formation is similar to the common ALD process and is described by two successive "half-processes". During the first half-process, the TMA reacts with the hydrogen atoms of the surface hydroxyl groups through a ligand exchange in which an O−Al bond is formed and methane is released. The formation of highly dense and full coverage dielectric layer requires that the binding sites, hydroxyl groups, densely cover the entire surface. To this end, oxygen plasma is generated outside the chamber and injected to it to react and produce high coverage of hydroxyl groups. This is especially critical when depositing on metals, such as gold, where the formation of surface hydroxyl groups are not thermodynamically favorable[34] (Supporting Information, Figures S4 and S6). Following this in situ surface preparation step, a predetermined amount of the TMA molecules' vapor is injected into the reaction chamber. The driving force for the TMA injection, being the pressure difference between the TMA antechamber (1 Torr) and the reaction chamber (being held below 0.02 Torr), results in a relatively dense and uniform injection aimed to promote faster reaction with the exposed surface. The surface reaction, the ligand exchange,[35] involves a single hydroxyl group (eq 1a) or two hydroxyl groups simultaneously (eq 1a) and results in a methyl-terminated surface.[36] In the second half-process described in eq 2, H_2O is introduced to the reaction chamber in the same way as described for the TMA. The H_2O reacts with the methyl-terminated groups, releasing methane, and reconverts the surface population back to hydroxyl-terminated groups; see the process flow at Figure 1 part b and c. Thus, the H_2O/TMA is a self-terminated process by nature, adding up to a single layer per cycle with an approximated thickness of 1.2 Å,[32] enabling to

determine film thickness with atomic-scale accuracy, independent of reaction time or amount of reactants.



$$\| \mathrm{Al{-}OH} + \mathrm{Al(CH_3)_3}\,(g) \rightarrow \| \mathrm{Al{-}O{-}Al(CH_3)_2} + \mathrm{CH_4}\,(g) \quad (1a)$$



$$2\| \mathrm{O{-}}H + \mathrm{Al(CH_3)_3}\,(g) \rightarrow (\| \mathrm{O{-}})_2\mathrm{AlCH_3} + 2\mathrm{CH_4}\,(g) \quad (1b)$$

$$\| \mathrm{Al{-}CH_3} + \mathrm{H_2O}\,(g) \rightarrow \| \mathrm{Al{-}OH} + \mathrm{CH_4}\,(g) \quad (2)$$

To deduce on the quality of the modified ALD process and the resulting film characteristics we initially examined the layer structural properties using high-resolution transmission electron microscopy (HRTEM). Films were covered by epoxy as part of the TEM sample preparation procedure. The HRTEM micrograph of 50-deposition-cycles film, shown in Figure 2a, reveals three distinct layers under the epoxy cover. The first two lower layers are the thermally deposited polycrystalline aluminum substrate and the overlaying oxidized region, the latter partly formed during the predeposition plasma exposure. The oxidized Al region is distinguishable as it preserves some of the crystallinity of the aluminum film. The third layer is the MVD100E tool-deposited AlO_x film which appears to be amorphous as is common to low temperature deposition processes. An important use of the HRTEM images is to accurately calibrate the ellipsometry measurements. To this end we examined the cross sections of a second film, 100-deposition-cycles thick, to fix two points on the ellipsometry scale. The extracted films thickness for the 50- and 100-cycles films were 5.9 ± 0.4 and 12 ± 0.4 nm, respectively, with an additional 2 ± 0.5 nm of plasma oxidized alumina.

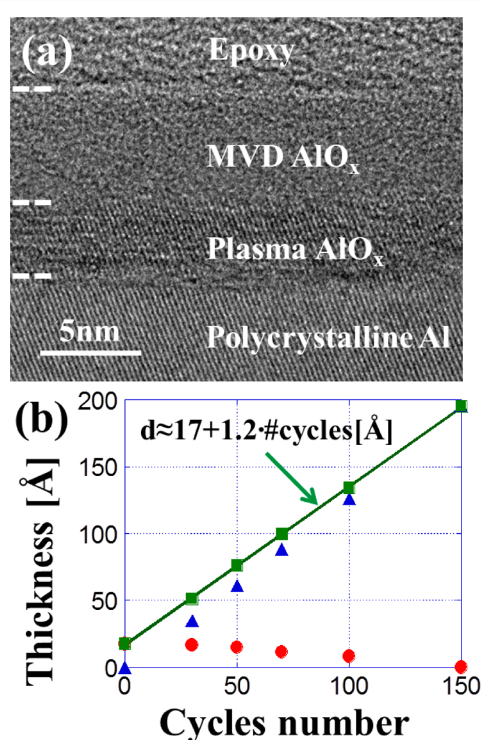


Figure 2. (a) HRTEM cross section of an AlO_x-MVD deposited film. (b) Ellipsometry measurement distinguishing the oxygen plasma induced AlO_x (circles) and the MVD-deposited AlO_x (triangles).The sum of both is indicated with squares.

The HRTEM-calibrated ellipsometry measurements of samples prepared at 60 °C, shown in Figure 2b, confirm the linearity of the film growth process (square symbols). We note that the process may also be performed at lower temperatures, and a range of samples prepared at temperatures between 40 and 100 °C demonstrated similar properties (not shown here). Using ellipsometry one can also attempt to differentiate between the crystalline and amorphous films and extract their thickness individually (triangles and round symbols in Figure 2b). However, this procedure failed for the thick alumina layers where it could not reproduce the ∼2 nm crystalline alumina that was clearly evident in the HRTEM images. The average values obtained by fitting the linear slope are 17 Å of oxidized aluminum and a growth rate of 1.2 Å/cycle, in agreement with literature predicted values.[32]

After establishing the structural characterization and quality of the layers when grown on Al substrates, we turned to explore their electrical properties. To this end we measured leakage current, breakdown field, and capacitance using a metal−insulator−metal (MIM) configuration. The structure was prepared by first depositing a large area aluminum film on a glass substrate followed by the above layer by layer process to grow the desired AlO_x film thickness. Finally, a top aluminum layer was deposited (thermal evaporation) through a shadow mask resulting in several capacitors on a given substrate (see Supporting Information, Figure S2). To ensure reliable interpretation of the measured data we tested very different capacitor areas (10^{-4} cm^2 and 2.52×10^{-2} cm^2) and in some of the samples we also replaced either the top or bottom aluminum electrode with gold.

Figure 3a presents the leakage current density as a function of applied electric field obtained for AlO_x layer thicknesses, which, according to Figure 2b, correspond to values between ∼29 and ∼137 Å. We also added the result obtained for the oxidized aluminum only (∼17 Å thick). To compare the different thicknesses and observe potentially enhanced leakage or breakdown in the thinnest films, we plotted the current as a function of electric field and not bias voltage. But for the oxidized aluminum-only layer, all other capacitors showed good insulating properties which are similar up to 7.5 MV cm^{-1}. We note that the thinnest layer, with layer by layer deposited thickness of 12 Å (+∼17 Å oxidized aluminum) demonstrated somewhat higher leakage currents but similar robustness toward breakdown. The breakdown electric field (not shown) was slightly above 8 MV cm^{-1}. However, for the application considered here, 3 MV cm^{-1} is already a high enough electric field and is equivalent to about 60 V across 100 nm SiO_2 film. The similarity between the leakage curves points toward the very good insulating properties of the layers. In the literature such good insulating properties of oxide layers are associated with low density of oxygen vacancies,[37] an effect that is supported by the layers' stoichiometry, Al_2O_x ($x > 3$), obtained by XPS bulk measurements (Supporting Information, Figure S5).

Turning to the capacitance measurements, the round symbols in Figure 3b show the capacitance as a function of the layer thickness (d). As described in the Supporting Information capacitance was deduced from both voltage and frequency-dependent capacitance measurements, where the values presented correspond to the high frequency (1 MHz to 1 kHz) capacitance (Supporting Information, Figure S3). The solid line in Figure 3b represents the $1/d$ dependence expected from an ideal capacitor, and it clearly shows that the data

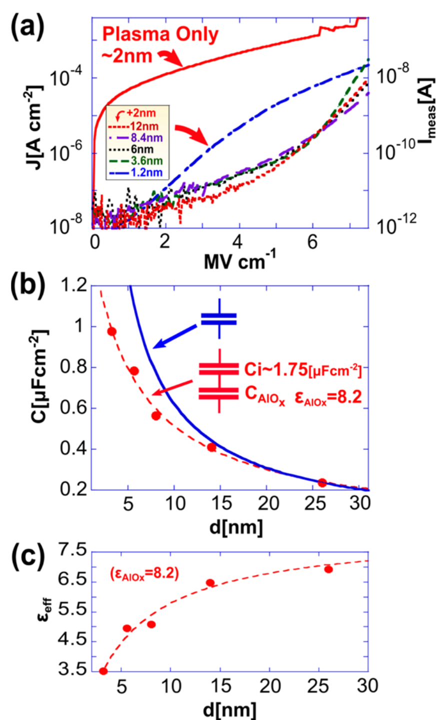


Figure 3. MIM electrical characterization. (a) Leakage current density as function of applied electric field; the indicated thicknesses do not include the additional plasma induced oxide layer with the approximated thickness of 17 Å. (b) Capacitance measurements (red circles), and the fit (dashed line) to the serial capacitance model, compared to the ideal model of a single capacitor (solid line). (c) Effective permittivity as function of insulator thickness.

cannot be reproduced by an ideal single capacitor. The analysis of thin and ultrathin parallel plate capacitors often deviates from the classical analysis, which follows $1/d$ and theoretically approaches infinity capacitance as thickness is reduced. The reasons for this deviation can be attributed to quantum effects[38,39] at the metal−insulator interface or to the formation of an interfacial layer which introduce yet another capacitor in series.[34,40,41] The inclusion of interface capacitance is abundant in analyses of capacitors films when their thickness ranges between 2 nm and 25 nm. In such a case the measured capacitance, C_{meas}, is said to be composed of both the interface capacitance, C_i, and the film capacitance according to

$$1/C_{meas} = 1/C_i + d/\varepsilon_{AlO_x}\varepsilon_0 \tag{3}$$

In eq 3, d is the insulator thickness and ε_0 is the vacuum permittivity. Following previous works on thin films,[40] we fitted the experimental values to eq 3, dashed line, resulting in an interface capacitance of $C_i = 1.75[\mu F\ cm^{-2}]$ and bulk dielectric constant of $\varepsilon_{AlO_x} = 8.2$. For completeness, we note that the results in Figure 3b can also be reproduced by an effective dielectric constant that decreases for thinner films, see Figure 3c. In Figure S4 of the Supporting Information, we show that the measured capacitance is dependent on the type of metal used for the capacitor plate and hence we favor the interpretation through the existence of a serial interface capacitor. Regardless of the mechanism at hand it places another scaling limit on reducing the dielectric film thickness.

Before presenting the effect of the thin AlO_x on the VOFET performance, we briefly discuss the architecture and operation of such FETs so that the structural and functional roles of the gate dielectric are better understood. As shown in Figure 1, in the VOFET architecture, the layers are vertically stacked. The spacing between the source and the drain, which defines the channel length, is determined by the OSC thickness, a parameter easily downscaled in fabrication. Featuring intrinsically short channel length, the VOFET is able to drive high current density under low applied drain bias. Thus, it offers a facile fabrication method for low-power devices. However, the physical principles underlying the VOFET behavior differ from those of lateral FETs.[19,42] As previously described in ref 42 and recently discussed in depth in ref 18, the channel, being vertical, is not directly influenced by the gate. Instead, the gate alters the charge injection properties of the source−OSC interface. When unbiased, the source−OSC Schottky barrier dominates the current between the source and the drain. The current can then be described similarly to the current at a contact limited (CL) diode. By applying gate bias, the resulting electric field induces a potential barrier lowering, ultimately resulting in space charge limited (SCL) conduction (ref 19 section IV.E). The gate influence penetrates its way to the source−OSC interface region through gaps in the metallic patterned electrode (see Figure 1i), which would have been otherwise completely screened because of the atomic length of the Debye shielding in metals.[43] Taking a closer look at the mechanism that facilitates this switching behavior,[18] we note that the potential barrier lowering induces charge accumulation at the patterned source electrode perforations. As the charge injection into the channel is confined within the perforations, both it and the electric field screening are greatly affected by the patterned electrode perforations' (also referred to as "tunnels") aspect ratio through the so-called "tunnel effect".[42] It is worth noting that gate screening effects by the source electrode, are more dominant in the vertical configuration than in the lateral one, a fact that stands behind the original design of the perforated source electrode.[44] Still, minimizing the gate screening and increasing the gate's capacitance bear consequence on important functional parameters, such as the subthreshold swing. In previous work, we dealt with the patterned electrode screening effects[18,19] and have shown that it is necessary to realize an ultrathin and smooth patterned electrodes with determined perforation diameter size, for practical use (see Supporting Information of ref 32, Figures S2 and S3). In this study, we keep the patterned electrode design fixed, and concentrate on the influence of the gate capacitance.

We demonstrate the gate capacitance effect by comparing two structures, one with a standard bottom gate, 100 nm thermal grown SiO_2 dielectric, and a second, which has a structured bottom gate and ~8 nm AlO_x dielectric. An image of a structured back gate VOFET is shown in Figure 1j. As mentioned above, to isolate the effect of the dielectric thickness reduction, and thus mostly the effect of the increased dielectric capacitance, the remaining of the structure was kept the same. To that end, we rely on the fabrication process in which the perforations' aspect ratio is determined through block-copolymer (BCP) based self-assembly and lift-off processes. These processes are schematically shown in Figure 1 steps d through g and are thoroughly described in refs 9 and 18.

The deposition of ultrathin BCP solution to result in the required pattern formation[45] is directly related to the substrate surface energy, that is, its hydrophilic/hydrophobic nature. The as-deposited AlO_x contact angle with H_2O and the one reached at steady state after a number of days are 23° and 33°, respectively (see Figure 4a and b and ref 46). These values

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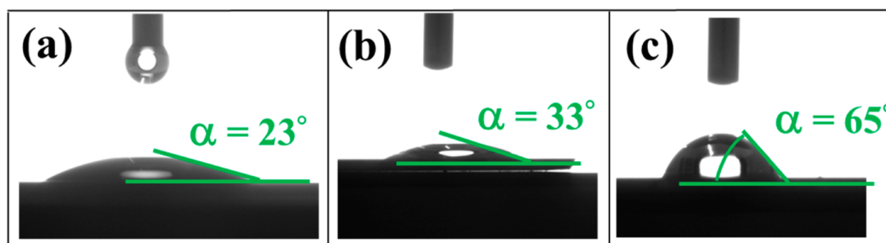

Figure 4. H_2O contact angle measurements: (a) bare AlO_x layer immediately after deposition, (b) bare AlO_x layer 3 days after deposition, and (c) after hydrophobic solutions treatment.

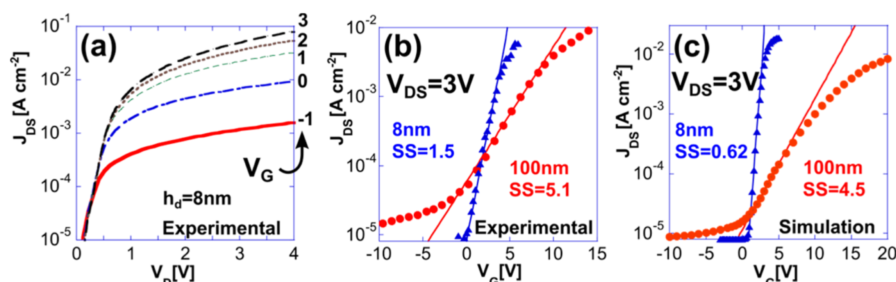

Figure 5. VOFET operational characterization. (a) Output characteristics (J_D−V_{DS}) of the MVD dielectric based VOFET. (b) Comparison of the transfer characteristics (J_D−V_{GS}) of the two structures: MVD dielectric-based (triangles) and 100 nm SiO_2-based (circles) PE−VOFET. (c) Simulation comparison between the transfer characteristics of two VOFETs with different dielectric thicknesses.

indicate a very hydrophilic surface which would cause dewetting of the hydrophobic BCP solution and thus prevent the formation of the required thin (sub 50 nm) films. Tuning this value to be compatible with the BCP self-assembly process is done through soaking the substrate in hydrophobic solutions such as acetone resulting in an increased contact angle of 65° (Figure 4c). Through this method, the obtained perforation diameters were approximately 80 and 60 nm, over SiO_2 and AlO_x, respectively.

For the purpose of metal deposition the AlO_x surface provides excellent adhesion allowing for reliable electrode formation down to below 10 nm, as required by this transistor architecture.[42] The good insulating properties of the AlO_x produced by the modified process allowed us to avoid the often required step of covering with organic SAM and thus maintain the good adhesion of the oxide surface and thus the robustness of the metals (Ti/Au) constituting the patterned electrode to the insulating stack. This is especially important where the fabrication process relies on a lift-off process that may damage very thin metal films where adhesion is not perfect (as adhesion to SAM may be). Patterned electrodes fabricated over the oxide layer with thicknesses down to ∼7 nm demonstrate sheet resistance of ∼280 Ω sq^{-1}, which decreases to ∼110 Ω sq^{-1}, when the thickness increases to ∼9 nm (details on the patterned electrodes thickness vs transparency and conductivity are available in ref 18)

To complete the device structure, 500 nm C_{60} fullerene and top Al drain contact are used with the two platforms, the one with the SiO_2 and the one with the AlO_x dielectric. Pin-hole formation in the fullerene film prevents further thickness downscaling (this probably because of the effect of the modulated perforated surface on the semicrystalline C60 film). However, one can use amorphous semiconductors, as was shown in ref 13, demonstrating reliable structures with sub-100-nm channel lengths, with the prospects of downscaling to few tens of nm. Since our focus here is on the gate dielectric, we do not include study of other semiconductor materials that would indeed allow for very thin channel lengths.

Figure 5a shows the output characteristics of the device made with the thin alumina layer. The device demonstrates switching within gate bias range of 3 V, and high driving current of over 10 mA cm^{-2} under drain bias below 2 V. As Figure 5a and to some extent also Figure 5b shows the transistor is not OFF at zero gate bias and a negative bias is required to obtain better ON−OFF ratio. As is discussed in detail in ref 18 and 42, this is associated with nonideal alignment between the electrode work function and the C_{60} LUMO level (i.e., too low injection barrier). Figure 5b shows the transfer characteristics of devices of the two types, being driven by source drain bias of 3 V. To quantify the difference between the performance of both we use the definition of the subthreshold slope (SS) [$\Delta V_{GS}/\Delta\log(J_{DS})$]. The SS value measures the gate bias change required to increase the current between the source and the drain by one decade. The SS value is extracted from the transfer characteristics, $\log(J_D)-V_{GS}$ plot, at the region between V_{On} and V_T (Supporting Information, Figure S8). This value decreases from ∼5.1 V/dec for 100 nm SiO_2-based devices (Figure 5b, circles) to ∼1.5 V/dec for the MVD-based devices (Figure 5b, triangles).

Compared to what is achieved in lateral FETs upon reducing the oxide thickness, one might expect a higher reduction in the slope by the factor of $(d_{SiO_2}/\varepsilon_{SiO_2})/(d_{AlO_x}/\varepsilon_{eff}(d))$ = 17 instead of just 3.5. As discussed in ref 19, this is, at least in part, due to the unique architecture if the vertical device, which makes the slope or the on/off ratio limited also by the aspect ratio of the perforations (metal film thickness relative to perforation typical width). To gain some intuition as to the extent of the ideal influence of downscaling the dielectric layer thickness, we have utilized a mean field self-consistent numerical simulation prepared in MatLab. Description of the simulation is found in ref 19 and specific simulation parameters are found in the Supporting Information, Figure S7 and Table S2. Figure 5c shows the transfer characteristics obtained by the simulation for

devices with 100 and 8 nm thick dielectric layers. The SS values derived from these curves (4.5 and 0.6) show a factor of 7.5, which is still significantly smaller than the factor of 17 expected based on performance of lateral FETs. There is still a difference between the experiment and the numerical results, which may be due to either the model not being able to capture all the physics (see discussion in ref 19) or due to the presence of trap states at the interface between the AlO_x and the semiconductor. Further research in this direction, involving trap state passivation is required to elucidate this issue.

■ CONCLUSIONS

We have presented a low temperature technique for the formation of reliable, oxide-only, pinhole free, high-k insulating layers with atomic scale thickness accuracy based on a layer-by-layer self-assembly process that is slightly modified compared to the commonly used ALD process. Regardless of the layers' thickness the leakage properties as a function of applied electric field were found to be identical, allowing the usage of ultrathin layers (sub-8-nm) with capacitance ranging between 0.5 and 1 μF cm^{-2}. Our initial studies of the film structure showed oxygen rich stoichiometry that may attribute to the excellent insulating properties. To demonstrate its use, we further incorporated these layers as the gate dielectric of a PE-VOFET, benefiting from the ease of controlling the dielectric's surface properties to allow the block-copolymer-based self-assembly fabrication. The PE-VOFET is intrinsically characterized by low-power consumption; through integrating the thin AlO_x layer, we demonstrated a low-power as well as low-voltage PE-VOFET as it operates under low V_{GS} bias. Considering the low temperature processes described here, we further note that this device may be readily made flexible with a simple change of substrate material. The prospects of the vertical architecture for efficient integrated circuits,[13] as well as the properties of the demonstrated modified layer-by-layer self-assembly AlO_x dielectric for large area electronics, place them both, individually or combined, as interesting components for organic logic as these elements commence their way into commercial implementations.

■ EXPERIMENTAL SECTION

Device Fabrication. Devices were fabricated over highly doped p-type silicon wafers with 100 nm, dry, chlorinated thermal oxide layer (purchased from Nova Electronics Materials), which served as the bottom gate and dielectric layer of the reference PE-VOFETs, and as the substrate for the AlO_x-based VOFET. Samples were cleaned with a nitrogen gun and rinsed in acetone, methanol, and isopropanol solutions, sequentially, for 5 min each, in ultrasonic bath and finally dried over a hot plate at 110 °C. Al bottom contacts, for MIM (on glass) and VOFETs (on silicon substrates), were deposited to the thickness of 30 nm by e-gun evaporator (Temescal, FC-1800) and patterned using shadow masks. AlO_x dielectric was deposited to the required thickness by a Molecular Vapor Deposition machine (MVD100E, Applied Microstructures Inc.). Prior to deposition the Al bottom gate was treated in situ with mild (remotely generated) oxygen plasma (15 s, 150 W), which was followed immediately by the MVD100E deposition process. The number of MVD100E cycles varied between 10 and 200 according to the desired film thickness. In each cycle, the reactants were vaporized and introduced into the reaction chamber for a period of 1 s before being thoroughly removed by nitrogen purging. Polystyrene (PS) masks were produced according to the procedure previously described in ref 9 using self-assembly of polystyrene-block-poly(methyl methacrylate) (PS-PMMA) diblock-copolymer (BCP) (M_n 941 kDa, 33 wt % PS, purchased from Polymer Source, Inc.). Patterned source electrodes were formed by a sequential deposition (TFDS-184, VST systems Ltd.) of a thin titanium layer (nominally 3 nm, serving as adhesion layer) and gold layer (approximately 6 nm). The metal film deposition was followed by a lift off process resulting in the patterned electrode (PE). Further PE-VOFET fabrication steps were performed in a nitrogen inert atmosphere glovebox. C_{60} fullerene 99.9% n-type OSC (purchased from MER Corporation) was thermally evaporated over the PE under vacuum conditions of ~10^{-6} mbar to a nominal thickness of 500 nm. Finally, Al top contact, the drain electrode, was thermally deposited on top.

Electrical Characterization. Leakage current measurements, I_D–V_D sweeps, were performed for the MIM analysis on several samples (≥5 samples from each thickness) using a Semiconductor Parameters Analyzer (SPA; Agilent 4155B). Capacitance was measured at 1 MHz on the same samples, using a capacitor analyzer (Boonton, 7200 capacitancemeter). The complex impedance was measured as a function of the frequency (from 1 MHz to 1kHz) using an AC spectroscopy system, a frequency response analyzer coupled to an electrochemical test interface (Novocontrol Alpha-AK and POT/GAL). Data was analyzed using the Zview software (Scribner Associates, Inc., U.S.A.). Electrical characterization of the PE-VOFETs was performed with Semiconductor Device Analyzer (Agilent B1500A) in a glovebox in dark.

Structural Characterization. PE-related fabrication steps (layers thickness, perforation diameter, etc.) and the AlO_x film roughness were characterized by an AFM system (Veeco DI-3000) in tapping mode. HRTEM analysis was performed with the Titan 80–300 kV S/TEM (FEI) and served to calibrate ellipsometry measurements. HRTEM sample preparation was performed in a Gatan 691 Precision Ion Polishing System (PIPS). The AlO_x thickness analysis was performed by an ellipsometry measurement (VASE, J. A. Woollam Co., Inc.). AlO_x stoichiometry was measured with X-ray Photoelectron Spectroscopy (XPS; Thermo VG Scientific Sigma Probe). Surface adhesion properties were characterized through evaluation of the surface energy, based on contact angle measurements (Ramé-hart model 250 Standard Contact Angle Goniometer).

■ ASSOCIATED CONTENT

Supporting Information

Details on structural characterization using AFM and XPS. The layout of the MIM configuration is shown, as well as details on the two methods used to extract capacitance values. A comparison between Al and Au electrodes at the MIM configuration is shown as well as the Au films' contact angle measurements. Computational model and simulation parameters used in this study are detailed. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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ABBREVIATIONS

OFET = organic field effect transistor
OSC = organic semiconductors
PE-VOFET = patterned electrode vertical organic field effect transistor
MVD = molecular vapor deposition
ALD = atomic layer deposition
TMA = trimethylaluminium
MIM = metal−insulator−metal
PE = patterned electrode
BCP = block copolymer
CL = contact limited
SCL = space charge limited
AFM = atomic force microscopy
TEM = transmission electron microscopy

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